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16. (AMENDED) The method according to claim 15, wherein the step of [optimizing said sequence of spread spectrum] selecting said ROM codes further comprises the sub-steps of:

(A) initializing a phase lock loop (PLL) at power supply ramping;

(B) stabilizing said PLL with spread spectrum modulation turned off;

(C) loading said sequence of spread spectrum ROM codes;

(D) switching on spread spectrum modulation;

(E) recording transient behavior of said clock signal until PLL is in spread spectrum steady-state;

(F) switching off spread spectrum modulation;

(G) recording transient behavior of said clock signal until spread spectrum modulation is completely off;

(H) comparing recorded transient behavior to predetermined criteria;

(I) if the recorded transient behavior does not meet said predetermined criteria, shifting said sequence of spread spectrum ROM codes, wherein a last ROM code is moved to a first position and remaining ROM codes are shifted one position forward;

(J) if the recorded transient behavior meets said predetermined criteria, finalizing said sequence of spread spectrum ROM codes; and

(K) repeating sub-steps (D) through (J) until said recorded transient response meets said predetermined criteria.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicants' representative thanks Examiner Yeh for the indication of allowable matter.

DOUBLE PATENTING

The rejection of claims 1-8 and 12-13 under the judicially created doctrine of double patenting has been obviated by the attached terminal disclaimer and should be withdrawn.

OBJECTION TO THE SPECIFICATION

The objection to the specification has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claim 16 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-2, 4-5, 12-15 and 18-19 under 35 U.S.C. §102(e) as being anticipated by Hardin et al. (U.S. Patent 6,292,507) has been obviated and should be withdrawn.

The earliest priority date Hardin et al. is entitled to is the filing date, September 1, 1999. Attached to this response is a declaration under 37 C.F.R. 1.131 providing evidence that the present invention was conceived and reduced to practice prior to September 1, 1999. Since the invention date of the present invention precedes the filing date, 35 U.S.C. §102(e) does not apply. As such, the rejection under 35 U.S.C. §102(e) should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 9 under 35 U.S.C. §103(a) as being obvious over Hardin et al. in view of Sha '646 has been obviated and should be withdrawn. Claim 9 depends on claim 1, which is now believed to be allowable. While Applicants' representative does not necessarily agree that Sha '646 is a valid art reference, since Hardin '507 is not a valid reference (as described above in light of the attached declaration), the rejection is moot.

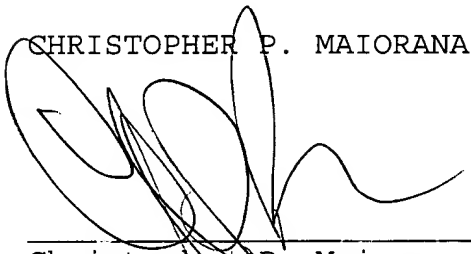
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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Please replace the paragraph beginning at page 3, line 18 with the following paragraph:

Referring to FIG.1, a block diagram of a circuit 10 illustrating a conventional phase lock loop based spread spectrum clock generator is shown. The circuit 10 generates a signal OUT in response to (i) a reference signal REF and a command signal SSON. The signal REF is presented to an input prescaler 12 and a multiplexer 14. The signal OUT is presented to a feedback prescaler 20 and a multiplexer 22. The signal SSON is presented to (i) the control inputs of the multiplexers 14 and [20] 22 and (ii) the spread spectrum circuitry 26. In response to the command signal SSON, (i) the multiplexer 14 selects between the reference signal REF and an output of the input prescaler 12, (ii) the multiplexer 22 selects between the output signal OUT and an output of the feedback prescaler 20 and (iii) the spread spectrum circuitry modulates the signal out.

Please replace the paragraph beginning at page 4, line 11 with the following paragraph:

Referring to FIG. 2, a timing diagram and an oscilloscope tracing illustrating signals of the circuit 10 are shown. The

timing diagram illustrates that a transition 30 in the signal SSON results in an immediate transition at the control inputs of the multiplexers 14 and 22 [20]. A portion 40 of the oscilloscope tracing illustrates the large transient response of the circuit 10 when spread spectrum modulation is switched on.

Please replace the paragraph beginning at page 9, line 16 with the following paragraph:

The circuit 114 generally comprises, in one example, an input prescaler 140, a multiplexer 142, an input divider 144, a phase lock loop (PLL) 146, a feedback prescaler 148, a multiplexer 150, a feedback divider 152, a spread spectrum circuit 154, and a ROM 156. The signal REF is generally presented to an input 158 of the input prescaler 140 and an input 160 of the multiplexer 142. An output 162 of the input prescaler 140 is generally connected to an input 164 of the multiplexer 142. The signal SSON_A is generally presented to a control input 166 of the multiplexer 142. An output 168 of the multiplexer 142 is generally connected to an input 170 of the input divider 144. An output 172 of the input divider 144 is generally connected to an input 174 of the PLL 146. The signal FDBCK is generally presented to an input 176 of the [input divider 144] PLL 146. The PLL 146 may be configured to generate the signal CLK.

Please replace the abstract with the following paragraph:

A circuit and method for controlling a spread spectrum transition are presented comprising a first circuit and a second circuit. The first circuit may be configured to generate a clock signal in response to (i) a reference signal, (ii) a sequence of spread spectrum ROM codes, and (iii) a command signal. The second circuit may be configured to synchronize [said] the command signal to a feedback signal. The sequence of spread spectrum ROM codes may be generated according to a predetermined mathematical formula and optimized in accordance with predetermined criteria.